David Sarnoff Research Center
Subsidiary of SRI International

CERAMIC/METAL COMPOSITE CIRCUIT-BOARD-LEVEL TECHNOLOGY FOR APPLICATION SPECIFIC ELECTRONIC MODULES (ASEMs)

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Certificate of Technical Data Conformity

The David Sarnoff Research Center hereby certifies that, to the best of its knowledge and belief, the technical data delivered herewith under Contract No. DAAB07-94-C-C009 is complete, accurate, and complies with all requirements of the contract.

Date: 6/10/96

Certifying Official: _____

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per AD-A305371

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Section I
WBS Task 2.2: Customize LTCC-M for Specific Applications

A. TASK OBJECTIVE

Extend the LTCC-M technology to meet any requirements of the technology demonstration modules, and any general packaging trends of the electronics industry.

B. INTRODUCTION

Progress is reported in the area of extending LTCC-M to higher density circuits. To increase the circuit density of LTCC-M substrates, thick film inks have been developed that can produce test structures having 4 mil diameter vias and 4 mil lines and spaces. This pattern routes one or more 4 mil lines between 4 mil diameter vias. Reliability testing of a high density test pattern featuring 4 lines and spaces combined with 4 mil vias is reported.

C. HIGH DENSITY CONDUCTOR PATTERNS

A second set of high density test boards (4-layer boards with 9 daisy chains interconnecting a total of 978 vias; 4 mil diameter vias and 4-5 mil wide lines) were fabricated using green tape punched with 4 mil diameter holes and with the following materials: ABT-52 green tape; INJ-202B via ink; BC-110 buried conductor ink and TC-10 top conductor ink. The high density via patterns were injection filled. None of these parts were defect free due to defects in the screens and also imperfect buried conductor prints; these problems resulted in discontinuities within the chains.

Three parts from this group were subjected to temperature cycling (-55 to 125°C, 30 min. holds at temperature) and three parts were subjected to 150°C temperature aging; the resistance of each daisy chain was monitored as a function of test cycles or hours. A summary of the test parts and total test cycles or hours that each part underwent is given in Table I.1. For the most part, only negligible or no variations in chain resistance were observed in parts tested for >600 temperature cycles and aged for up to 1610 hours at 150°C. Typical results for temperature cycling and temperature aging tests are shown graphically in Figures I.1 and I.2. In this test pattern, chain #s 1-3 are high density chains (4 mil diameter vias on 16 mil centers with (1) 4 mil wide line between vias; 120 vias per chain); chain #s 4-6 are medium density chains (4 mil diameter vias on 30 mil centers with (2) 5 mil wide lines with 5 mil spaces between vias; 120 vias per chain); and chain #s 7-9 are low density chains (4 mil diameter vias on 42 mil centers with (3) 5 mil wide lines with 5 mil spaces between vias; 84 vias/chain).

A third group of test parts is now being fabricated using corrected screens and an improved buried conductor ink, comprised of a fine Ag powder (no flake).

Table I.1 - Test Part Summary

Part ID	Test	Total Test Hrs. or Cycles	# chains tested per board
B1	Temp. Cycling	628 cycles	6
B2	Temp. Cycling	602	9
B4	Temp. Cycling	590	9
B3	150°C Temp. Aging	1610 hrs.	9
B5	150°C Temp. Aging	1610	7
B6	150°C Temp. Aging	1372	4

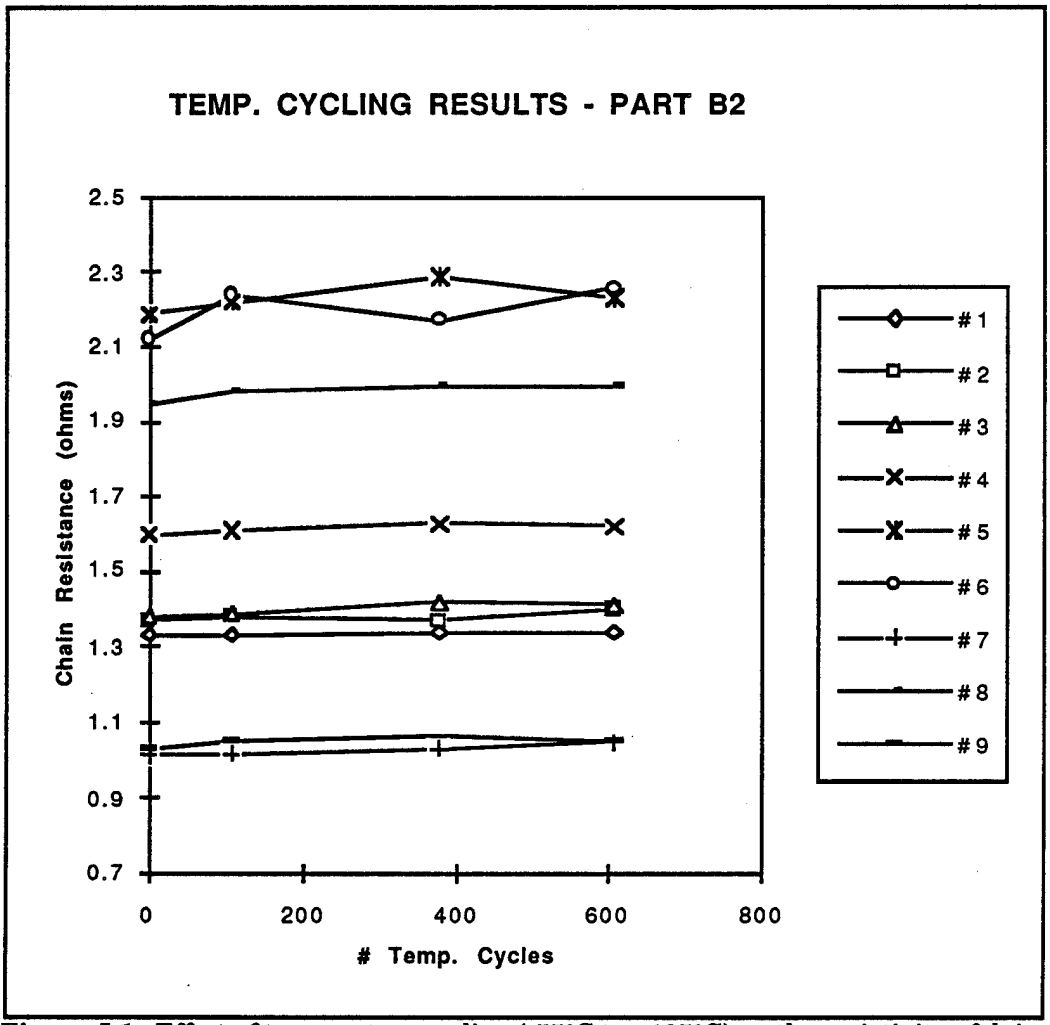


Figure I.1: Effect of temperature cycling (-55°C to +125°C) on the resistivity of daisy chains for sample B2.

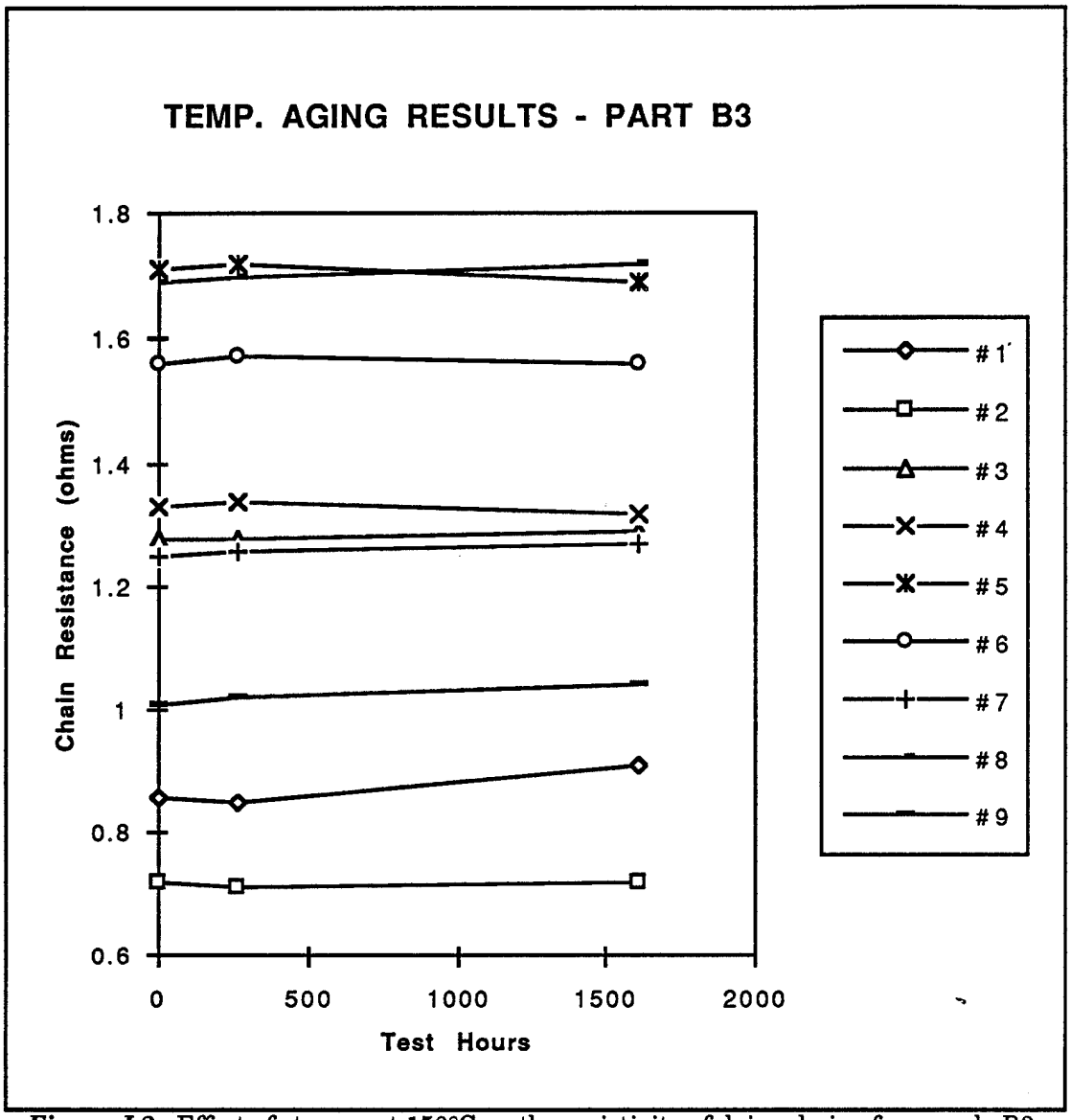


Figure I.2: Effect of storage at 150°C on the resistivity of daisy chains for sample B3.

D. PLAN FOR NEXT QUARTER

- Continue reliability testing of 4 mil via test structures
- Fabricate additional daisy chain test patterns having 4 mil vias connected to 4 mil lines with 4 mil spaces with a corrected set of screens
- Continue reliability testing of Ag thick film top conductors

Section II
WBS Task 2.3: Fabrication and Testing of Technology Demonstration Modules

A. TASK OBJECTIVE

The objective of this task is to design, fabricate, assemble, and test 4 different technology demonstration modules. These modules are: (1) an optoelectronic transceiver module, (2) a power amplifier package, (3) an advanced PCMCIA card, and (4) a Power Electronic Building Block (PEBB).

B. INTRODUCTION

The four technology demonstration vehicles planned for this program were chosen because each module had clear military applicability, and also met the requirements of the consumer marketplace. Table III.1 shows the application of each demonstration module to the needs of the US armed forces.

Table III.1:
Military Relevance of LTCC-M Technology Demonstration Vehicles

Prototype Application	Supporting Co.	Type	Military Relevance
Advanced PCMCIA Card (ORBCOMM Modem)	Torrey Science	Mixed Signal Module	1. Similar electronics needed for global tracking of high value and critical military materials and components (e.g. armaments) 2. Supports DoD: • Materials Command • Logistics Command • Transportation Command • "Total Asset Visibility" program 3. Technology applicable to the following: • NSA (R2) dual function PCMCIA card • Trackers • Message Terminals • CESEL • Special Forces replacement of high frequency radio systems (miniaturization) • Global extension of communications in Force 21 "Digital Battlefield" 4. Applies to Military Global Mobile Information Systems
High Power Motor Controller (Power Electronics Building Blocks)	Harris	High Power Single Chip Package	1. Supports US Navy Contract # N-00024-94-C-4088 (an Advanced Tech. Demo. with Naval Sea Systems Command) 2. Computer controlled Integrated Variable Speed Electric drive for ships (surface and subsurface) and tanks 3. Computer controlled Electric Actuators for airplanes, ships, and tanks 4. Auxilliary Power Unit Generators, Solid State Power Controllers for airplanes 5. Power Inverters and Converters for ships and airplanes
Optoelectronic Transceiver Module	AMP	MCM	1. Supports the construction of low cost broadband networks at military bases and installations. 2. Such networks support: • ATM based switching architectures • Transfer of large amounts of graphical and multimedia data • Digital signals • Encrypted signals 3. Supports ARPA contract "Manufacturable Low Cost Single-Mode Bi-directional Links for Fiber in the Loop Optical Networks" • Currently LTCC-M is the sole technology for this application
Power Amplifier Packages (microwave)	Raytheon	GaAs single chip package	1. Portable government cellular communications systems and wireless LANs 2. Applies to Military Global Mobile Information Systems

A general set of LTCC-M design guidelines has been communicated to all the circuit designers. Sarnoff has been closely working with all circuit designers to develop manufacturable designs.

C. OPTOELECTRONIC TRANSCEIVER MODULE

Under this program Sarnoff, and AMP will develop a package that will integrate an optoelectronic MCM, an optical fiber, several silicon devices, and several passive components. This program provided bare-board tested LTCC-M packages to AMP (for module assembly) in May, 1996.

To meet the various design configurations of AMP, two similar packages were designed and fabricated together in a multi-up format. The decision to fabricate the "A" and "B" designs together minimizes the overall NRE costs for building this package. The revised package designs, shown in Figure III.1(a) and (b), were signed off by AMP. After conversion into an AutoCad file, hard tools were designed and screens were fabricated.

1. Challenges of this package

- Use of large area solid ground planes and shielding structures on all layers for noise immunity
- Crosstalk minimization
- Need for high precision cavities to minimize bond wire length of the high speed interconnections, especially the 1.2 Gbit/sec link
- Need for a high thermal conductivity base for laser stability and thermal management
- Package must be hermetic

2. Package Statistics

Size: 0.54" x 1.10"

Components interconnected: Optoelectronic MCM, 2 bare ASICs (Si), resistors and capacitors

Interconnect density: general design with 8 mil lines/spaces and 8 mil diameter vias; 6 mil lines and spaces in the bond pad areas.

Number of layers: 3

Number of vias: 258

Number of component mounting cavities: 2

Number of nets: 26

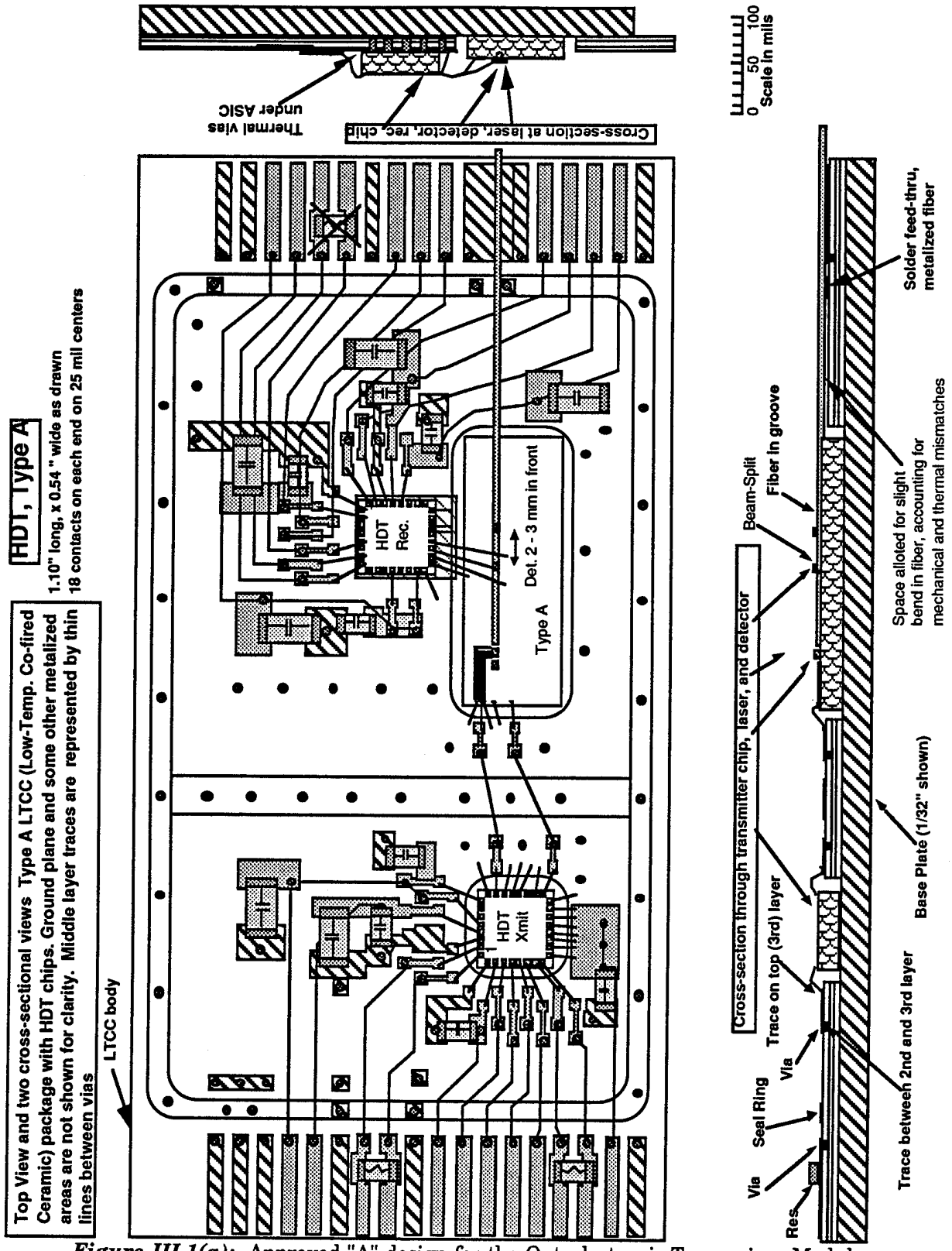


Figure III.1(a): Approved "A" design for the Optoelectronic Transceiver Module.

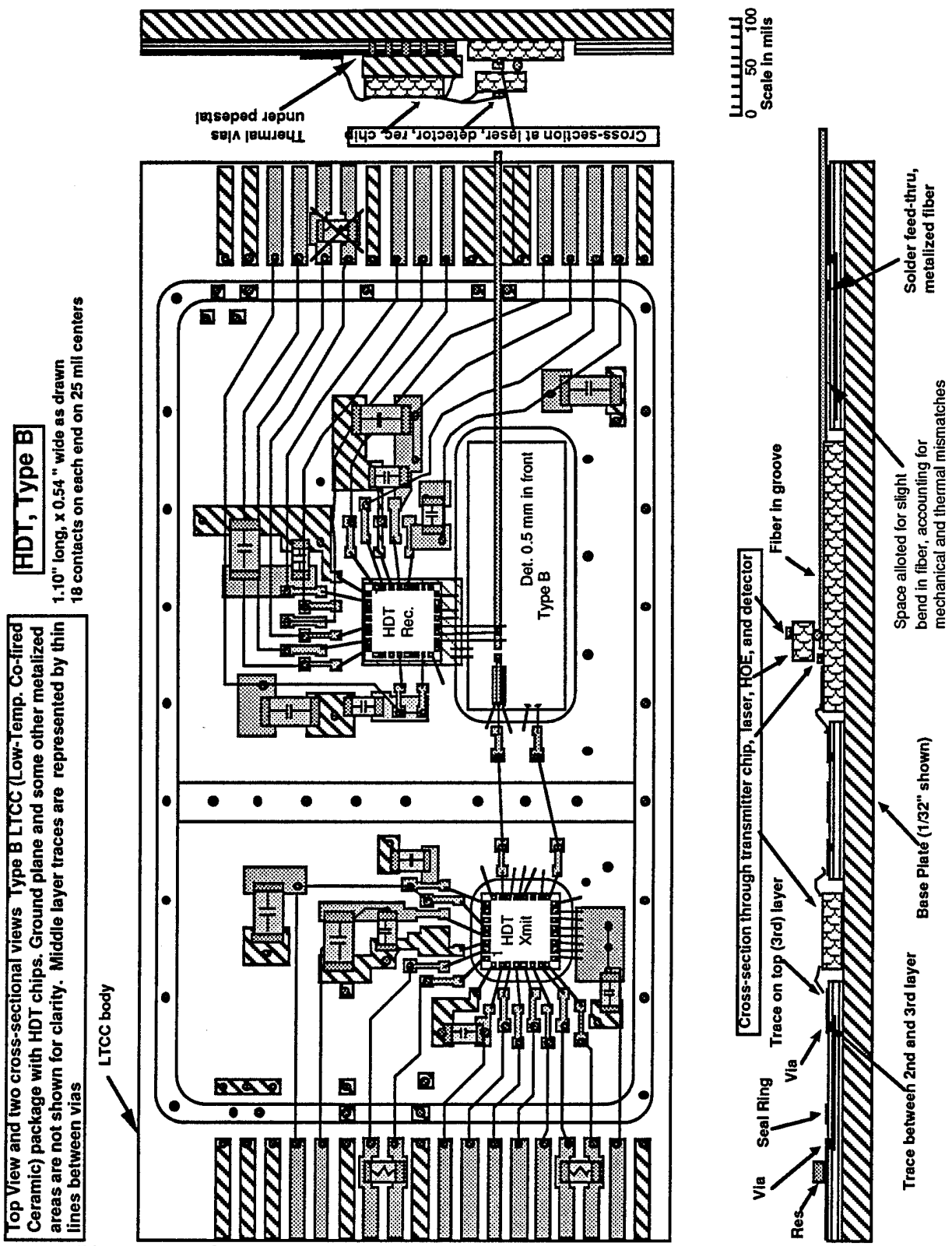


Figure III.1(b): Approved "B" design for the Optoelectronic Transceiver Module.

3. Package Fabrication

Based on the design furnished by AMP it was decided to build this package in a multi-up configuration (having both the "A" and "B" designs) using 3 layers of green tape that would attach to a 20 mil thick Cu/Mo/Cu base. All thermal vias would contact the metal base (not the metal bonding layer). The conductor pattern on the top layer of the package would plated by electroless Ni and Au plating baths. Finally, 63/37 eutectic Sn/Pb solder would be printed and reflowed to the seal ring area.

This required the design of 3 stencils (1 for each via layer), 5 printing screens (3 conductors, 1 bonding layer, 1 LN-1 layer), and 1 cavity punch (for punching all cavities simultaneously). Green tape formulation ABT-52 SC was cast about 8 mil thick for making these parts . After cutting into 3 1/4" squares it was sent to Schneider and Marquardt (Newton, NJ) for via punching. Vias for all layers were filled with thick film ink Via 253 using stencil filling techniques. All buried conductors were screen printed using thick film ink BC-103. The top conductor pattern was printed with ink TC-10, which after drying was overprinted with a fritless silver ink, BC-110. The use of a fritless silver overprint produces the best surface for wirebonding. To insure that the cavities maintained their "as punched" dimensions after firing, ink LN-1 was printed within the seal ring area, exposing only the bond pads.

After all screen printing was completed, the green tape layers stacked using pin alignment fixtures and then laminated. The lamination conditions were 3000 lbs and 185°F for 2 minutes. Next the cavities were punched into the laminated green tape stack. Then the green stack was co-laminated onto the previously prepared Cu/Mo/Cu core. Co-lamination conditions were 600 lbs and 185°F for 2 minutes. The packages were then fired in a 9 zone Lindberg belt firing furnace (air atmosphere) with a peak firing temperature of about 900°C.

After firing, the LN-1 material was removed by brushing with water. To smooth out the bonding pads, the top surface conductors were polished with a mildly abrasive slurry. Next the bonding layer in the cavities was stripped out by electrocleaning in a Patclin 303C bath. At this point the top surface conductors were plated by Pd activation, followed by a 5 - 10μm thick electroless Ni deposition, followed by a 8 - 10μin immersion Au deposition. At this point the boards were sent to Circuitest (Nashua, NH) for bare board testing (shorts and opens based on the netlist). Sixty circuits were tested, and the boards showed a first pass yield of 90%.

Solder (63/37 Sn/Pb) paste was then screen printed over the seal ring and then reflowed on a temperature controlled hot plate (230°C). After flux removal, the circuits were diced into individual packages using a composite material grinding wheel. Figure II.1 shows a tested package. Figure II.2 shows a package with a corner intentionally chipped away to expose the solid embedded ground planes, extending to within 5 mils of the package boundaries, required for electrical shielding. After final cleaning, the individual packages were shipped to AMP Inc. for module assembly and evaluation. Module assembly and testing are expected to start during the third quarter of 1996.

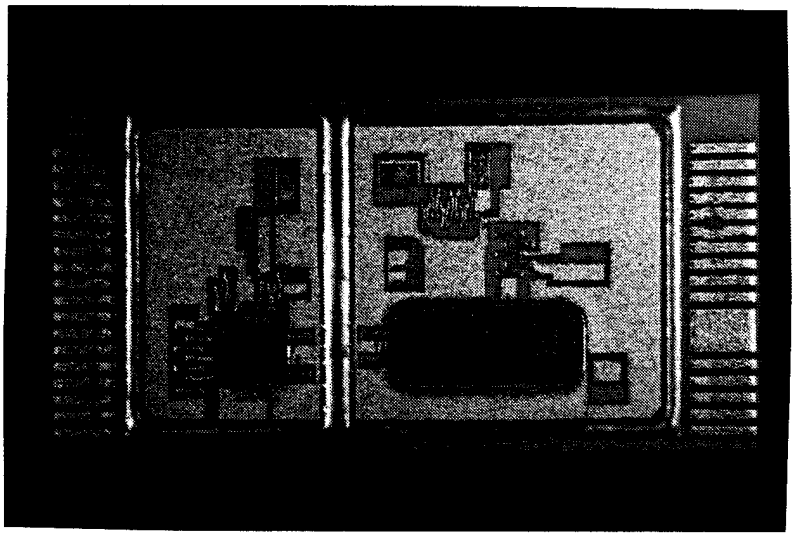


Figure II.1: An optical tranceiver package (0.54" x 1.1") fabricated using LTCC-M substrate technology.

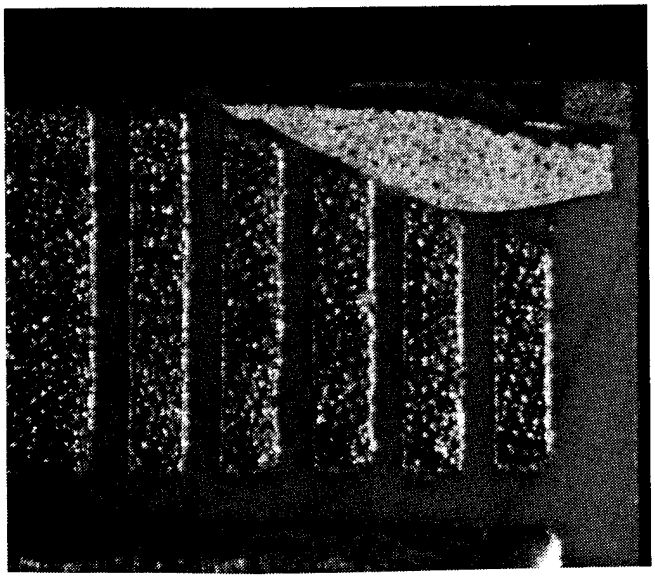


Figure II.2: An optical tranceiver package with a corner intentionally chipped away exposing solid ground planes extending to within 5 mils of package boundaries.

4. Lessons Learned

The primary cause of yield loss during bare board testing was shorts from bond pad locations. It was noticed during screen printing that there was some ink smearing from the BC-110 overprint. This can be corrected by designing a separate screen for the overprint that only contains the bond pads, and not the shielding. The shielding does not require any overprint. This was not done

during this first go-round because a "pads only" design was not supplied. Extraction of a "pads only" layer from the supplied AutoCad file would result in a significant delay, for a package whose design had already endured substantial delays.

D. POWER AMPLIFIER PACKAGE

The objective of this task is to design, fabricate, assemble and test a low cost power amplifier package for a GaAs microwave device. The package will be designed, assembled and tested by Raytheon and fabricated by Sarnoff.

1. Challenges of this package

- Low loss microwave package for operation at C-band frequencies
- Integral metal base to minimize "moding" effects
- Need for high precision, tiered cavities to minimize bond wire lengths from die to package
- Need for a high thermal conductivity base for 10 W power dissipation
- Thermal expansion match to GaAs for solder attachment of bare die to metal base
- Low loss transmission lines through seal rings

2. Technology Demonstration Vehicle

This technology demonstration vehicle, a C-band power amplifier package, was fabricated during this past quarter. A photograph of the package is shown in Figure II.3. The size of the Cu/Mo/Cu base is approximately 1" x 1". The C-band package requires a Type 3 cavity, a tiered cavity morphology where two separate laminates are stacked on top of each other with different cavity sizes. The cavity for the bottom laminate extends all the way to the Cu/Mo/Cu base. A GaAs FET and several microwave capacitors will be mounted in the cavity directly on the Cu/Mo/Cu.

The fabrication process is briefly summarized below:

1. Clean Cu/Mo/Cu base plate
2. Cut into 1" x 2.5" strips (each strip holds 2 circuits)
3. Plate Cu/Mo/Cu
4. Screen print all required layers on Cu/Mo/Cu
5. Punch via patterns (2 different patterns required)
6. Fill vias in all tape layers
7. Screen print all tape layers
8. Stack and laminate 3 bottom layers
9. Punch lower cavity pattern
10. Stack and laminate 3 top layers
11. Punch upper cavity pattern
12. Laminate all layers
13. Trim tape
14. Co-laminate tape layers to Cu/Mo/Cu
15. Fire in furnace
16. Electrolytic plate Ni and Au on Cu/Mo/Cu and all printed metal
17. Singulate

After singulation and final cleaning, the packages were sent to Raytheon for assembly and testing.

3. Lessons Learned

The Cu/Mo/Cu was prepared without any problems. However, during test lamination and firing trials, two problems were encountered. First, excessive sintering was observed in the silver conductor traces after firing. The ink was reformulated to increase the glass content, which in turn reduced the sintering. The glass content of this ink is the same as the silver inks used for fabricating the 50Ω seal ring feedthrough and the spiral inductor test structures. The necessary tape layers were reprinted with the reformulated ink. Excessive sintering was not observed with the reformulated ink. The second problem was conductor cracking after lamination and firing. Reducing the lamination pressure by 5 - 10% eliminated the cracking.

It was also discovered while making this module that the use of metal core contact ink, MC-4, affects the overall Ni-oxide properties. Normally, any exposed BX-M31 glaze can be readily removed by a chemical stripping operation after the LTCC-M part has been fired. However, when MC-4 is fired onto the metal core for the formation of contact pads, many exposed areas of glaze can no longer be easily removed by the chemical stripping process. This problem affected the cavities of the C-band power amplifier, where the exposed metal core required Au-plating for bare die and passive component attachment. For future packages, it is recommended that the silver thick film ink, MC-4 be printed in all areas where bare die will be soldered to the metal core.

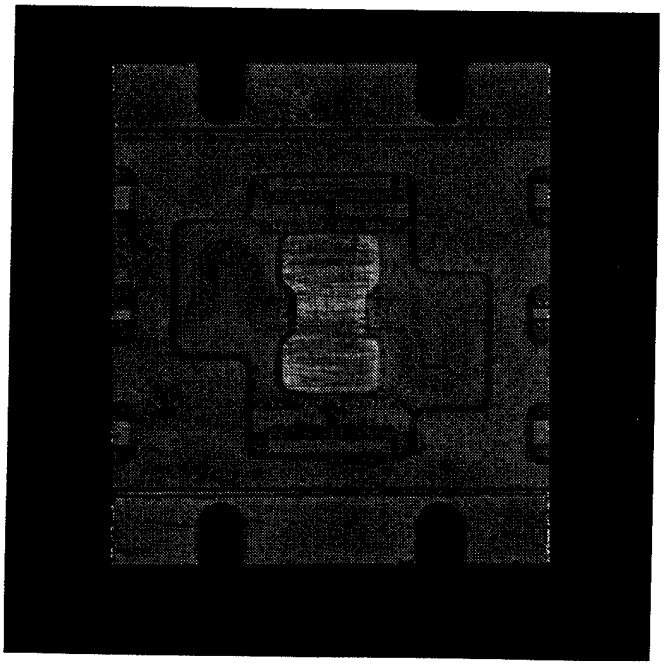


Figure II.3: C-band power amplifier package.

E. POWER ELECTRONIC BUILDING BLOCKS (PEBB)

1. Background

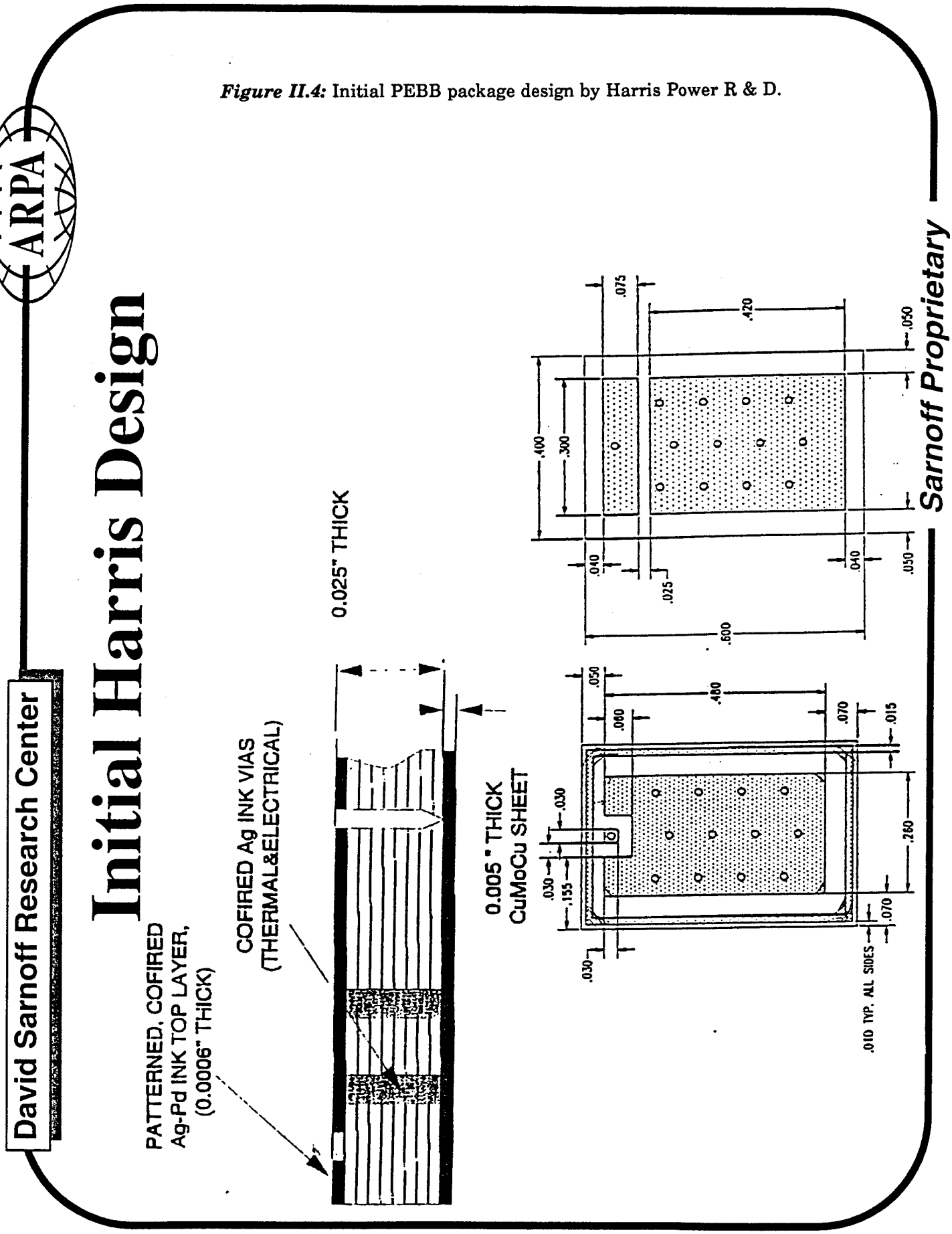
The objective of this task is to design, fabricate, assemble and test a low cost, PEBB "lid" in support of the U.S. Navy PEBB program, and to meet the packaging needs of high current semiconductor devices. PEBB "lids" are high power device substrates that connect the power device to its control signals on a printed wiring board, and also are part of the thermal management system that draws the heat away from the device (and the printed wiring board). This package will eliminate the need for traditional wirebonding for contact formation with external electrodes. This is also a significant improvement over the currently available plastic based power modules that have high parasitic inductance and resistance losses associated with wirebonding. In addition, reliability concerns regarding fatigue of bond wires and fracture of brittle semiconductor die under the stresses of the wirebonding process are also eliminated. The total device size is also reduced. The "lid" package will be designed, assembled and tested by Harris Power R & D and fabricated by Sarnoff.

The initial design provided to Sarnoff by Harris Power R & D is shown in Figure II.4. This design called for a thick film conductor on the top of the glass ceramic with 0.025" cofired thickness (two rectangular pads) and the Cu-Mo-Cu be etched to form a design calling for a rectangular guard ring, a small pad separated by a larger one with a 'U' neck. Twelve electrical/thermal through vias (0.015" dia.) in the larger pad and one in the smaller one will provide the necessary electrical and thermal characteristics demanded from this package.

2. Package Challenges

- Prevent camber in the LTCC-M board after cofiring with 0.005" Cu-Mo-Cu metal core and six layers of glass ceramic tape.
- Accommodate a very high density of vias over a large portion of the LTCC-M board, resulting from inherent design and multi-up of parts in a single board.
- Achieve good via contact through six layers of glass ceramic tape down to the metal core.
- Prevent cracking of the glass ceramic and cracks in the via material itself throughout the entire LTCC-M board.
- Devise and optimize the process for patterning the 0.005" Cu-Mo-Cu metal core by etching.

Figure II.4: Initial PEBB package design by Harris Power R & D.



3. Design Adaptation

The LTCC-M technology developed for Cu-Mo-Cu metal core was optimized for 0.008" diameter vias, whereas the initial Harris design called for 0.015" vias. In order to meet the required electrical properties, calculations made at Sarnoff and Harris suggested that many more vias (of 0.008" dia.) would be required, as opposed to 13 0.015" vias per package. The number of 0.008" vias necessary to meet the electrical properties was determined to be 58 per package (4 in the smaller pad area and 54 in the larger pad area). The final design of one package (unit cell) is shown in Figure II.5 with the modified dimensions, this is an X-ray view of the entire package. All of the 0.008" vias in the larger pads are on 0.024" centers.

The dimensions of LTCC-M packages for Cu-Mo-Cu was optimized on a 3" x 3" metal core. The PEBB package design called of a 0.400" x 0.600" package. This provided an opportunity to multi-up the number of such packages per LTCC-M board. It was determined that a 3 x 4 array of packages per board would be optimal. An x-ray view of the board layout is illustrated in Figure II.6.

4. Materials Adaptation

Twelve packages per board called for an extremely large number of vias (710 in total, 696 for twelve packages and 14 for fiducials). In addition to such high via density, all of the vias had to make contact from the top of the thick film Ag conductor pads down to the Cu-Mo-Cu metal core going through six layers of green ceramic tapes (to get a cofired thickness of the glass ceramic above 0.025"). The materials system needed to be adapted to achieve this task, each of which is briefly described below.

Tape Formulation : Six layers of ABT-52 tapes fired on a 0.005" thick Cu-Mo-Cu metal core did not minimize camber to acceptable levels. This called for a modification of the green tape formulation. The 'new' green tape formulation (ABT-61) slightly adjusted the component levels of the ABT-52 formulation. Six layers of ABT-61 tapes co-laminated onto 0.005" Cu-Mo-Cu metal cores gave "flat" fired LTCC-M boards necessary for preparing the multi-up PEBB packages.

Vias : Punching 710 vias per tape and hence 4260 vias per LTCC-M board (six such tapes per board), and deliver all packages from about 18 such boards, one by one, would be an enormously tedious process. The via punching done on other prototypes by an external vendor (Schneider & Marquard), based on their quotes, could not meet the program schedule. It was therefore decided to design a hard punching tool which will allow punching of all 710 0.008" diameter vias in one step in green ABT-61 tape. The tool was fabricated by an external machine shop.

Via filling with Ag-based inks in the ABT-61 green tapes punched by the hard tool was accomplished very successfully. Via ink (VIA 253) designed for this purpose gave excellent results, over 35,000 vias were filled (50 punched tapes) without a single miss in a single printing session. This excellent result is owed to a combination of the better quality of vias punched in a single step process and the optimized formulation of the via ink.

Figure II.5: X-ray view of the final design of the PEBB pacakage (one unit cell).

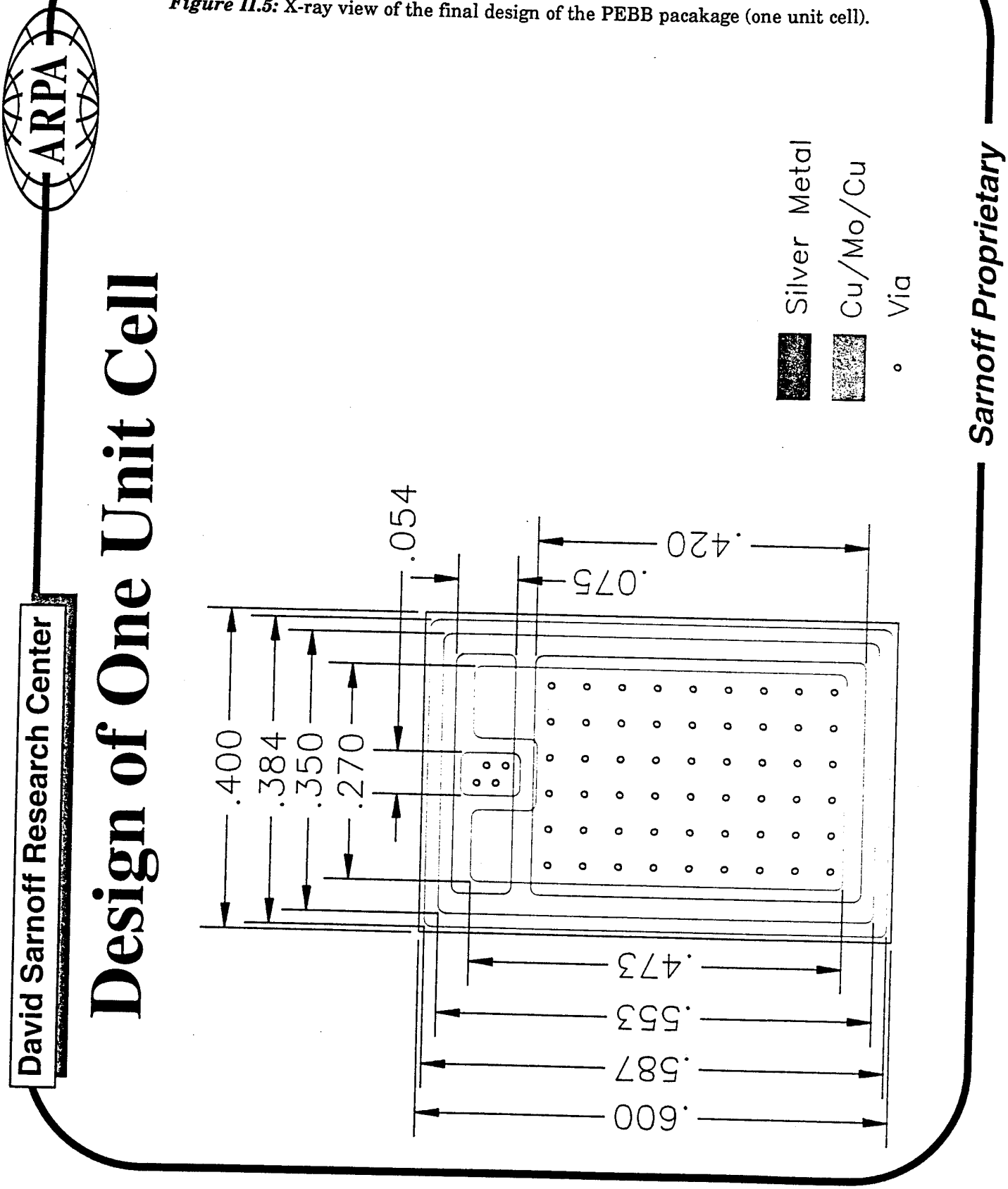
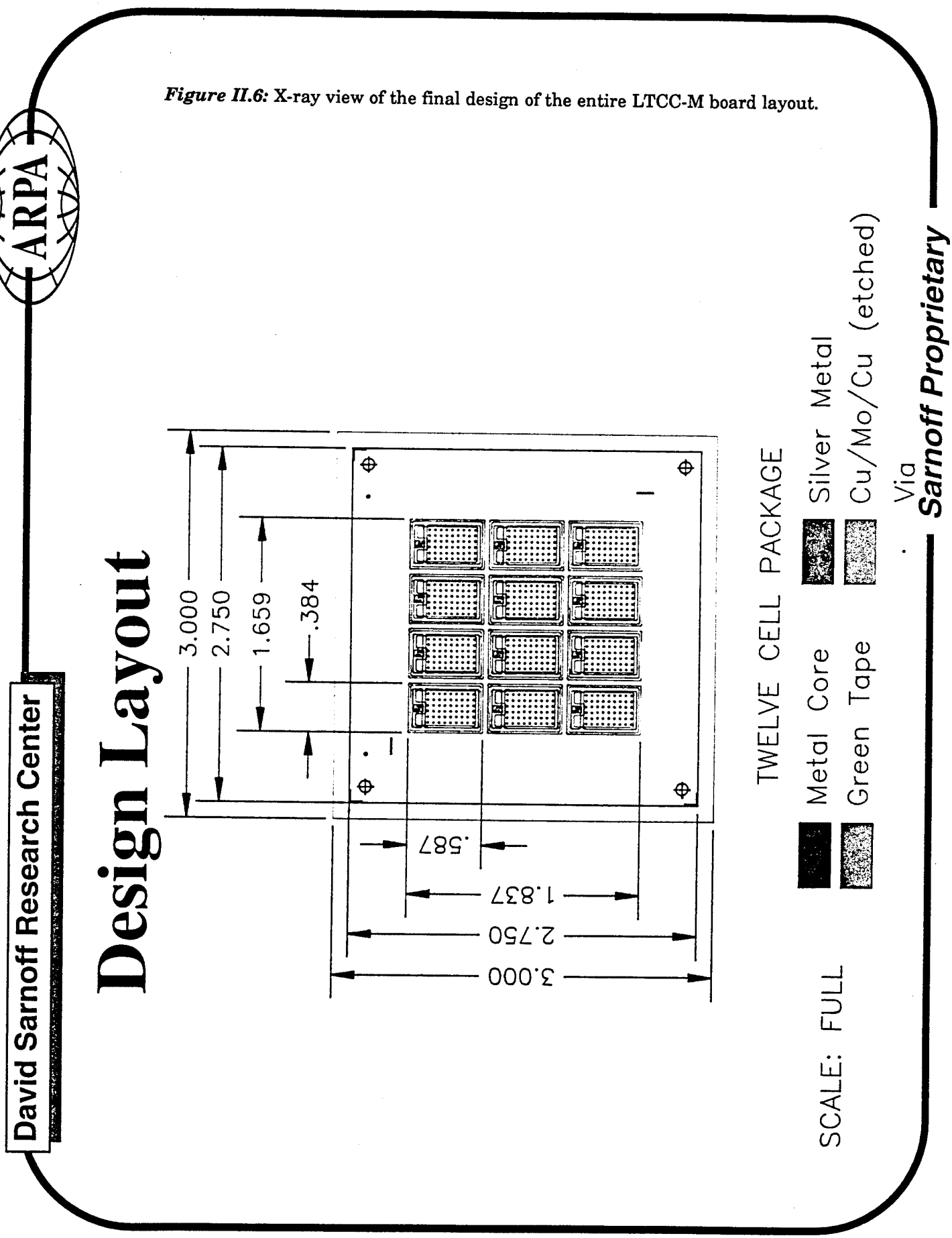


Figure II.6: X-ray view of the final design of the entire LTCC-M board layout.



A test board of the vias was fabricated in order to assess electrical continuity. A regular (0.020" thick) Cu-Mo-Cu metal core dotted with MC-4 silver ink (prepared earlier in the program) before Ni oxidation, was colaminated with a stack of six ABT-61 tape layers with vias filled and then cofired, see Figure II.7. Each and every of the 696 vias were tested for electrical continuity and every one of them in the test board gave satisfactory results.

Metal Core Preparation : Cutting 3" x 3" 0.005" thick Cu-Mo-Cu metal core by shearing (normal procedure) imparts inherent camber in the metal core, some of which is retained after cofiring. To further minimize camber (in addition to the ABT-61 formulation), the metal cores were cut by wire EDM. There was also a separate challenge to be met regarding perfect alignment of the metal core to the green tape laminate during co-lamination. The traditional optical technique used for colamination developed earlier in the program for via contact to metal did not have sufficient tolerance to align a very large number of vias for this prototype. It was determined that colamination be carried out in the Cu fixture itself that is also used for green tape stack laminations. To accomplish this, two holes (along the diagonal) were added to the metal core to mate with the alignment pins. Also two separate holes along an edge added to the metal core for high resolution optical alignment for photoresist deposition on the backside. All of these holes were drilled and then smoothed by wire EDM to 0.004" mil oversize in diameter to allow for Ni plating and subsequent oxidation. To minimize waste, the metal core (13" x 13" as received) was cut to 2.75" x 2.75" instead of 3" x 3".

The multi-up board with 710 0.008" diameter vias on 0.024" centers would minimize the amount of bonding glaze delivered to individual parts. After a few combinations of gaps in the bonding glaze, the optimum size of the opening in the glaze was determined to be a 0.016" square pattern on 0.024" centers and with the same centers as the vias. In order to minimize stresses in the firing of the glaze, a 0.010" gap (channel) was given exactly in the middle of all the twelve individual parts as illustrated in Figure II.8. After etching of Cu-Mo-Cu, this conveniently served as cutting keys for singulation. However, to print the glaze in such a sharp pattern, an especially viscous ink, BX-M31-6, was formulated.

The metal core preparation included the steps of silver dotting the metal core after Ni plating with MC-4 ink using a stencil which had 0.012" squares at the same centers as the vias. This was followed by firing the ink to the metal core. This was followed by printing the glaze BX-M31-6 and firing the glaze. BC-103 silver was then dotted using the via stencil and then dried, all of these steps are illustrated in Figure II.9 for one unit cell. TSOL-12 glue was applied prior to colamination.

ARPA

Via Continuity Test Board

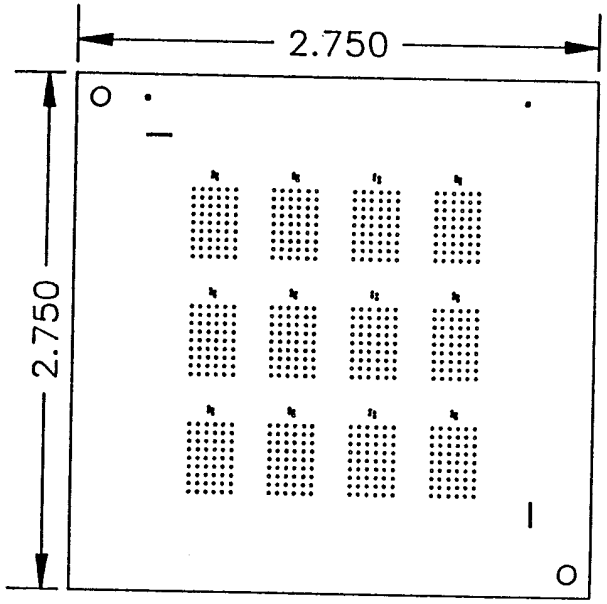
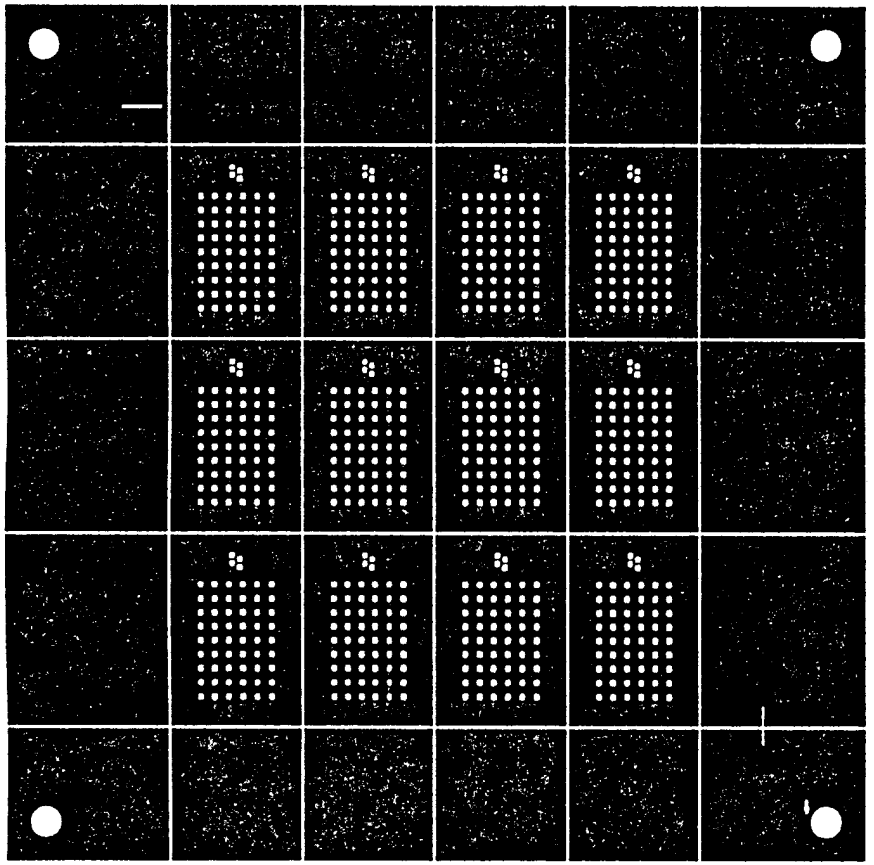


Figure II.7: Illustration of the cofired LTCC-M via test pattern board.

ARPA

Glaze Pattern

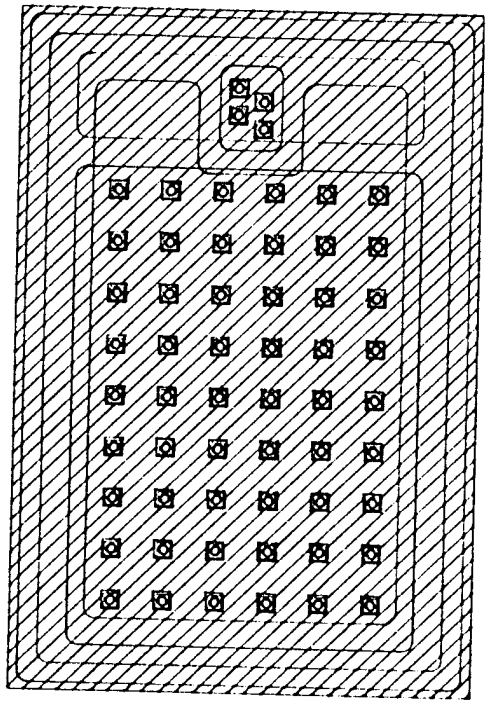


HARRIS SQ016 GLAZE

Figure II.8: Illustration of the glaze (BX-M31-6) pattern on metal core.

ARPA

Metal Core Preparation Steps



MC–4 Ag Ink (.012" sq)

BX–M31–6 Glaze (.016" sq)

Silver Metal

Cu/Mo/Cu (etched)

° Via

Figure II.9: X-ray view of various metal core preparation steps. Only one unit cell is shown in this figure.

Lamination & Colamination : Six layers of ABT-61 with all the vias punched and filled (with Via 253 ink) were stacked. The top conductor pattern was printed on the top tape in the stack with a newly formulated top conductor ink TC-9. The bottom side of the bottom most tape of the stack (the one that comes in contact with the metal core) was dotted with BC-103 with a stencil designed to do so. A tape of LN-1 was placed on the top of this six layer stack. Lamination was carried out using standard Cu fixtures at 3,000 LB load for a total of 2 min. after a 1 min. preheat at 185°F. Colamination was done by first putting the metal core in the fixture and then putting the laminate on top of it in the same fixture at 600 LB, also for a total of 2 min. after a 1 min. preheat at 185°F. Shearing was done after colamination to remove 0.125" from around each edge of the laminate. The part was then cofired and LN-1 tape washed off.

Gold Plating & Etching : A cofired part with LN-1 washed off was first subjected to standard nickel oxide stripping. The back side of the part, *viz.*, the exposed Ni side, was covered with a photoresist to develop a pattern for Au plating corresponding exactly to the etched pattern of Cu-Mo-Cu. A mask was designed to do so, such that after the photoresist deposition, Au was deposited by electroplating on both sides, the thick film and the Ni on Cu-Mo-Cu side was covered with gold corresponding exactly to the top and bottom pattern of the PEBB package. The Au on the metal core side can act as an etch mask by itself. However, in doing so there was significant undercutting during the etching process (up to 0.012"). This problem was minimized by designing an over sized photo mask, using this mask the photoresist was deposited on the electroplated Au on the metal core side and then the part was etched. The two mask configurations are illustrated in Figure II.10. The etching process needed to be optimized and the process now involves etching at 70°C for approximately 2 minutes. The etchant (described in last quarter's technical report) was a mixture of HCl, HNO_3 and H_2SO_4 diluted with distilled water.

Singulation : The dicing of the individual twelve parts from the etched LTCC-M boards involved mounting them on a plate using a wax and then cutting with a 0.015" thick blade. The cutting keys were already present by design of the glaze screen. After cutting, the parts were washed with organic solvents to clean off the wax. The entire singulation process was relatively rapid. Figure II.11 illustrates the two sides of a finished package.

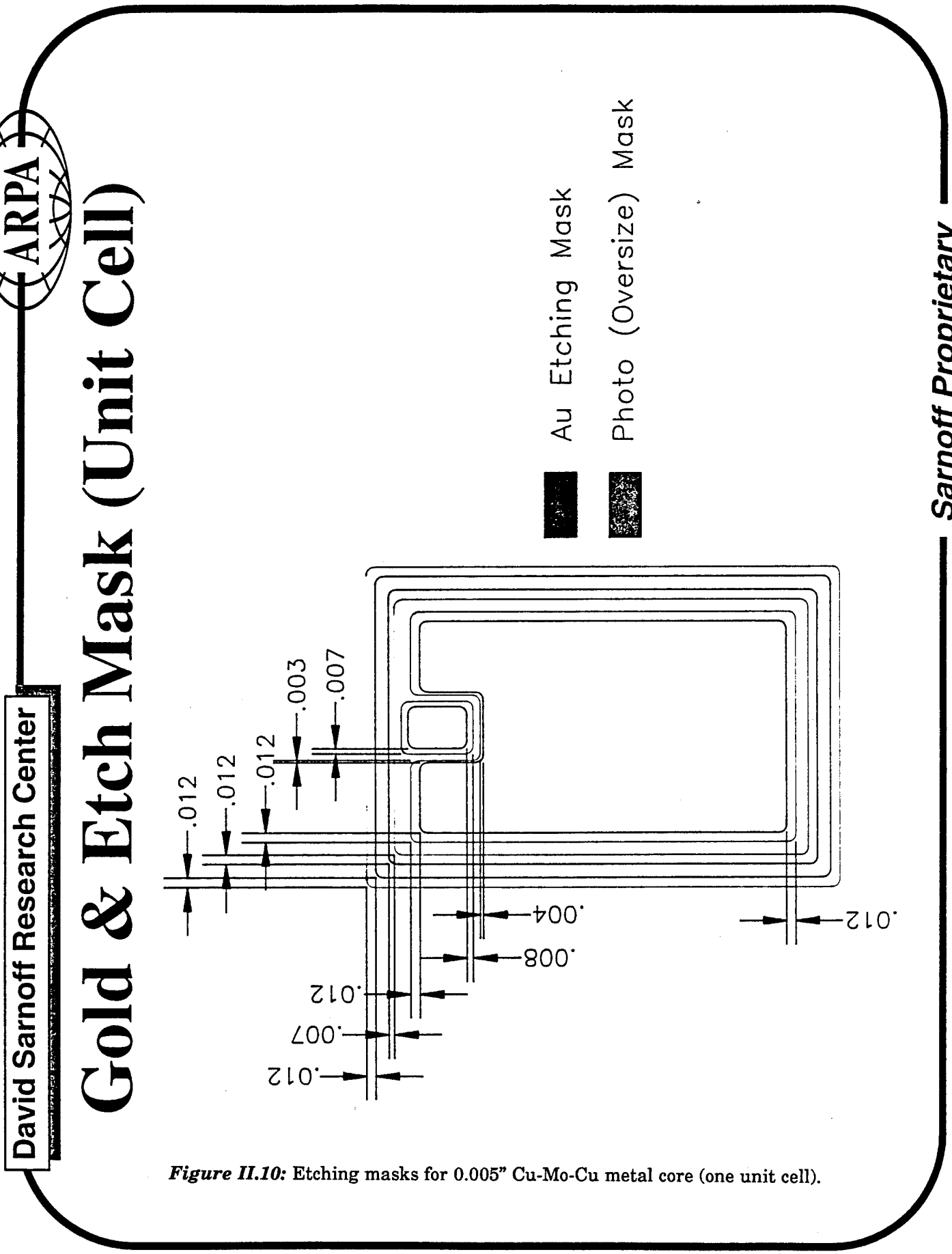


Figure II.10: Etching masks for 0.005" Cu-Mo-Cu metal core (one unit cell).

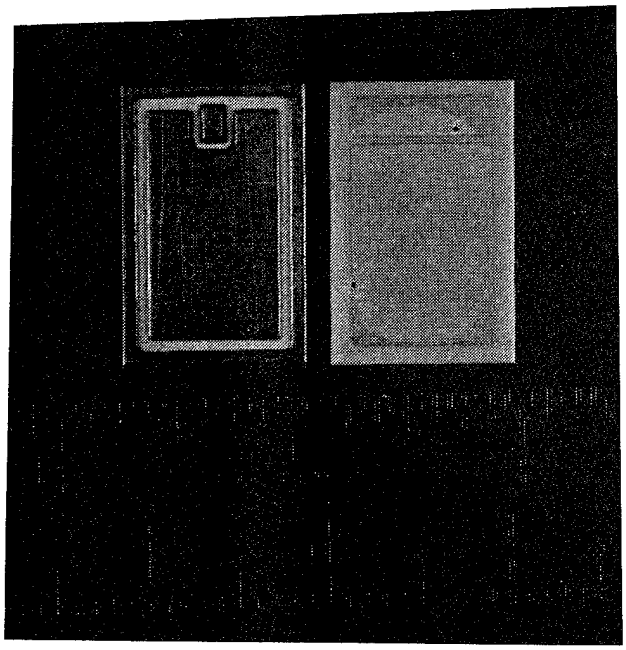


Figure II.11: Two PEBB package prototypes showing topside and bottomside metal patterns.

5. Summary of Results :

- Design adaptation of the PEBB completed.
- Materials adaptation involved adjustments in the green tape formulation, formulating glaze inks, top conductor inks and also adjustments in the cofiring temperature. All of these processes have been optimized.
- Development and optimization of the etching process completed.
- First set of samples of the PEBB package shipped to Harris Power R & D. Their initial evaluation results very encouraging.
- More parts are currently being fabricated to meet the total number of parts required for deliverables.

F. ADVANCED PCMCIA CARDS

Torrey Science is currently designing on RF Modem module based on an extended PCMCIA Type II card format. They have replaced SCI Systems with CTM, Microelectronic Packaging, Inc. as the module assembler because of SCI System's reluctance to build this module. CTM's expertise in building similar complex electronic modules was a key factor in their selection. The following is a summary status of this prototype design and fabrication:

- Torrey Science has already obtained or has commitment from IC vendors to supply all the active devices needed for this program.

- The module will utilize approximately 40 active devices including 16 different bare dice.

- Design and layout of the RF Modem module has been started.

- The details of the double-sided assembly required for this module will be dictated by the design. However, double-sided solder assembly trials were conducted at Sarnoff to verify materials-process compatibility. Good results were obtained with eutectic Sn-Ag as the high temperature solder and eutectic Sn-Pb as the low temperature solder.

G. PLAN FOR NEXT QUARTER

Optoelectronic Transceiver Module

- Module assembly by AMP
- Module evaluation by AMP

Power Amplifier Package

- Module assembly by Raytheon
- Module evaluation by Raytheon

Advanced PCMCIA Cards

- Complete design and layout at Torrey Science
- Begin substrate fabrication at Sarnoff

Power Electronic Building Blocks

- Module assembly by Harris
- Module evaluation by Harris

Section III
Important Findings

A. CUSTOMIZE LTCC-M FOR SPECIFIC APPLICATIONS

- High Density thick film silver test patterns with 4 mil lines and spaces and 4 mil diameter vias have shown no degradation during accelerated aging tests. These parts have survived more than 600 thermal cycles between -55°C and +125°C, as well as more than 1600 hours of storage at 150°C.

B. FABRICATION AND TESTING OF TECHNOLOGY DEMONSTRATION MODULES

- 30 Optical Transceiver packages have been delivered to AMP for module assembly and testing.
- 14 C-band Amplifier packages have been delivered to Raytheon for assembly and testing.
- Design adaptation of the PEBB completed.
- Materials adaptation involved adjustments in the green tape formulation, formulating glaze inks, top conductor inks and also adjustments in the cofiring temperature. All of these processes have been optimized.
- Development and optimization of the metal core etching process completed.
- First set of samples of the PEBB package shipped to Harris Power R & D. Results of their initial evaluation are very encouraging.
- More PEBBs are currently being fabricated to meet the total number of parts required for deliverables.
- Torrey Science has obtained commitments from IC suppliers for all active components (~ 40), including sixteen (16) different bare dice for fabrication of the Advanced PCMCIA Card Technology Demonstration Vehicle.
- Double-sided LTCC-M boards with surface mount packages on both sides have been successfully soldered at Sarnoff with an IR belt furnace, using eutectic Sn-Ag as the high temperature solder and eutectic Sn-Pb as the low temperature solder.

Section IV
Significant Developments

Thin film co-planar waveguide (CPW) test structures have been fabricated on top of LTCC-M substrates. Data has been measured up to 44 GHz, and all results are very encouraging for design and fabrication of 44 GHz low noise amplifiers to support the EKV Program, run by the U.S. Army. LTCC-M is the only substrate technology that can allow the fabrication of thin film CPW structures in a large area format, using materials that offer good circuit performance at mm-wave frequencies.

Section V
Plan for Further Research

CUSTOMIZE LTCC-M FOR SPECIFIC APPLICATIONS

- Continue reliability testing of Ag thick film top conductors
- Fabricate additional daisy chain test patterns having 4 mil vias connected to 4 mil lines with 4 mil spaces with corrected printing screens
- Continue reliability testing of 4 mil via test structures

FABRICATION AND TESTING OF TECHNOLOGY DEMONSTRATION MODULES

Optoelectronic Transceiver Module

- Module assembly and testing by AMP

Power Amplifier Package

- Module assembly and testing by Raytheon

Advanced PCMCIA Cards

- Complete design and layout at Torrey Science
- Begin substrate fabrication at Sarnoff

Power Electronic Building Blocks

- Complete delivery of all PEBB substrates
- Module assembly and testing by Harris

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The quarterly progress for the Ceramic/Metal Composite Circuit-Board-Level Technology for Application Specific Electronic Modules is described in this report. Data is reported for the following tasks: Customize LTCC-M for Specific Applications and Fabrication and Testing of Technology Demonstration Modules.

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